LIN CMOS™

OPERATIONAL AMPLIFIERS
TIMERS
AND
DATA ACQUISITION
CIRCUITS

DATA MANUAL

FIRST RELEASE EDITION
APRIL 1984

This booklet contains the data for the first Lin CMOS ™ products to be released using TI's silicon-gate CMOS process.

Lin CMOS technology offers the low power and high input impedance advantages of CMOS without the offset-drift and speed problems. The range currently comprises op-amps, a timer and two A/D convertors. This will be quickly expanded to cover comparators, power-supply controllers, line drivers and receivers, peripheral drivers and also more op-amps.

For more information on Lin CMOS technology and new products as they are released, please contact one of the TI sales offices listed on the back cover.

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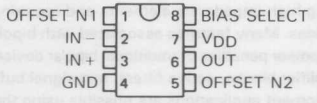
Lin CMOS is a trademark of Texas Instruments Incorporated

TYPES TLC251, TLC251A, TLC251B, TLC271, TLC271A, TLC271B
PROGRAMMABLE LOW-POWER LinCMOS™ OPERATIONAL AMPLIFIERS

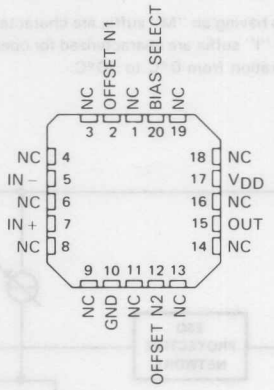
D2751, JULY 1983

- Wide Range of Supply Voltages:
  1 V to 16 V (TLC251)
  4 V to 16 V (TLC271)
- True Single Supply Operation
- Common-Mode Input Voltage Range Includes the Negative Rail
- Selectable Supply Current:
  Low = 10 μA Typ
  Medium = 150 μA Typ
  High = 1000 μA Typ
- Extremely Low Input Bias and Offset Currents:
  I_{IB}. . . 1 pA Typ
  I_{IO}. . . 1 pA Typ
- Low Input Offset Voltage. . . 2 mV Max
- Ultra Stable Input Offset Voltage:
  0.1 μV/Month Typ
  0.7 μV/°C Typ (Low Bias)
- Low Noise. . . 30 nV$\sqrt{\text{Hz}}$ Typ at 1 kHz (High Bias)
- High Slew Rate:
  High Bias. . . 4.5 V/μs Typ
  Medium Bias. . . 0.6 V/μs Typ
  Low Bias. . . 0.04 V/μs Typ

D, P, OR JG DUAL-IN-LINE PACKAGE
(TOP VIEW)



TLC271__M . . FH OR FK PACKAGE
(TOP VIEW)

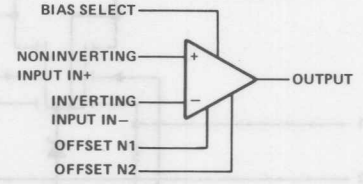


NC – No internal connection

description

The TLC251 and TLC271 are low-cost, low-power programmable operational amplifiers designed to operate with single or dual supplies. Unlike traditional metal-gate CMOS op amps, these devices utilize Texas Instruments silicon-gate LinCMOS™ process, giving them stable input offset voltages without sacrificing the advantages of metal-gate CMOS. This series of parts is available in selected grades of input offset voltage and can be nulled with one external potentiometer. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this family is ideally suited for battery-powered or energy-conserving applications. A bias-select pin can be used to program one of three ac performance and power-dissipation levels, from a high bias level (slew rate of 4.5 V/μs, power dissipation of 10 mW at a supply voltage of 10 V) to a low level (slew rate of 0.04 V/μs, dissipation of only 100 μW at 10 volts) to suit the application. The TLC251 offers the same operation as the TLC271, but also features guaranteed operation down to a 1 V supply. Both devices are stable at unity gain.

symbol



DEVICE TYPES, SUFFIX VERSIONS, AND PACKAGES

	TLC251	TLC271
TLC2__M	*	JG, FH, FK
TLC2__AM	*	JG, FH, FK
TLC2__BM	*	JG, FH, FK
TLC2__I	*	D, P
TLC2__AI	*	D, P
TLC2__BI	*	D, P
TLC2__C	D, P	D, P
TLC2__AC	D, P	D, P
TLC2__BC	D, P	D, P

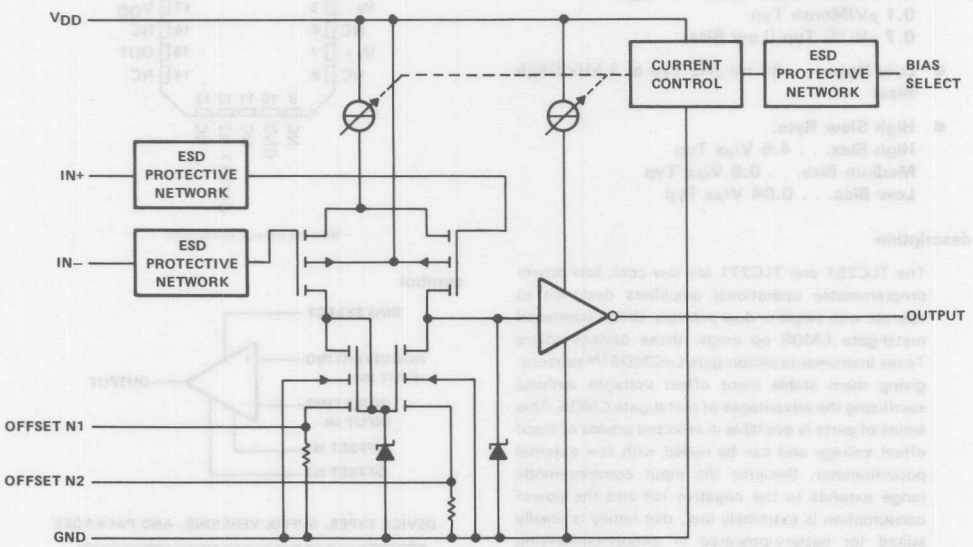
*These combinations are not defined by this data sheet.

TEXAS INSTRUMENTS

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC251 and TLC271 series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC271. Remote and inaccessible equipment applications are possible using the low-voltage and low-power capabilities of the TLC251. In addition, by driving the bias-select input with a logic signal from a microprocessor, these operational amplifiers can have software-controlled performance and power consumption. The TLC251 is well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications.

Devices having an "M" suffix are characterized for operation over the temperature range of −55°C to 125°C, those with an "I" suffix are characterized for operation from −40°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage range (any input) . . . . . −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . . unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)
D package . . . . . 725 mW
FH package (see Note 5) . . . . . 1200 mW
FK package (see Note 5) . . . . . 1375 mW
JG package . . . . . 1050 mW
P package . . . . . 1000 mW
Operating free-air temperature range: TLC271M, TLC271AM, TLC271BM . . . . . −55°C to 125°C
TLC271I, TLC272AI, TLC271BI . . . . . −40°C to 85°C
TLC251C, TLC251AC, TLC251BC,
TLC271C, TLC271AC, TLC271BC . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Table below.
5. For FH and FK packages, power rating and derating factor will vary with the actual mounting technique used. The values stated here are believed to be conservative.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	725 mW	5.8 mW/°C	25°C
FH	1200 mW	9.6 mW/°C	25°C
FK	1375 mW	11.0 mW/°C	25°C
JG	1050 mW	8.4 mW/°C	25°C
P	1000 mW	8.0 mW/°C	25°C

recommended operating conditions

		TLC251 TLC251A TLC251B			TLC271 TLC271A TLC271B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		1		16	4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1 V	0		0.2				V
	V_{DD} = 4 V	0		3	0		3	
	V_{DD} = 10 V	−0.2		9	−0.2		9	
	V_{DD} = 16 V	−0.2		14	−0.2		14	
Operating free-air temperature, T_A	TLC2__M				−55		125	°C
	TLC2__I				−40		85	
	TLC2__C	0		70	0		70	
Bias Select pin voltage		See application notes						

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		BIAS	TLC271_M			TLC271_I			TLC251_C, TLC271_C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC251_, TLC271_	V_O = 1.4 V, R_S = 50 Ω	25°C	Any			10			10			10	mV
				Full range				12			13			12	
		TLC251A_, TLC271A_		25°C	Any			5			5			5	
				Full range				6.5			7			6.5	
		TLC251B_, TLC271B_		25°C	Any			2			2			2	
				Full range				3			3.5			3	
α_{VIO}	Average temperature coefficient of input offset voltage			Full range	Low		0.7			0.7			0.7		μV/°C
					Medium		2			2			2		
					High		5			5			5		
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C	Any		1			1			1		pA
				Full range				3000			200			100	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C	Any		1			1			1		pA
				Full range				5000			300			150	
V_{ICR}	Common-mode input voltage range			25°C	Any	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage range‡		V_{ID} = 100 mV	25°C	Any	8	8.6		8	8.6		8	8.6		V
				Full range		7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	Low	30	500		30	500		30	500		V/mV
					Medium	20	280		20	280		20	280		
					High	10	40		10	40		10	40		
				Full range	Low	20	500		20	500		25	500		
					Medium	10	280		10	280		15	280		
					High	7	40		7	40		7.5	40		
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	Any	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	Low	70	85		70	85		70	85		dB
					Medium	70	85		70	85		70	85		
					High	65	82		65	82		65	82		
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C	Any		−55			−55			−55		mA
			V_O = 0, V_{ID} = −100 mV				15			15			15		
$I_{IH(SEL)}$	High-level input current to bias select		$V_{I(SEL)}$ = 0 V	25°C	High		10.5			10.5			10.5		μA
$I_{IL(SEL)}$	Low-level input current to bias select		$V_{I(SEL)}$ = 10 V	25°C	Low		1.3			1.3			1.3		μA
I_{DD}	Supply current		No load, V_O = 5 V, V_{IC} = 5 V	25°C	Low		10	20		10	20		10	20	μA
					Medium		150	300		150	300		150	300	
					High		1000	2000		1000	2000		1000	2000	
				Full range	Low			35			35			30	
					Medium			500			500			400	
					High			3000			3000			2200	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is −55°C to 125°C for TLC2__M, −40 °C to 85°C for TLC2__I, and 0°C to 70°C for TLC2__C. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.

‡The output will swing to the potential of the ground pin.

electrical characteristics at specified free-air temperature, V_{DD} = 1 V

PARAMETER			TEST CONDITIONS†		BIAS	TLC251_C MIN	TLC251_C TYP	TLC251_C MAX	UNIT
V_{IO}	Input offset voltage	TLC251C	V_O = 0.2 V, R_S = 50 Ω	25°C	Any			10	mV
				0°C to 70°C				12	
		TLC251AC		25°C	Any			5	
				0°C to 70°C				6.5	
		TLC251BC		25°C	Any			2	
				0°C to 70°C				3	
α_{VIO}	Average temperature coefficient of input offset voltage			0°C to 70°C	Any		1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C	Any		1		pA
				0°C to 70°C				100	
I_{IB}	Input bias current		V_O = 0.2 V	25°C	Any		1		pA
				0°C to 70°C				150	
V_{ICR}	Common-mode input voltage range			25°C	Any	0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	Any		450		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C	Low		20		V/mV
					High		10		
CMRR	Common-mode rejection ratio		R_S = 50 Ω, V_O = 0.2 V, V_{IC} = V_{ICR} min	25°C	Any		77		dB
I_{DD}	Supply current		V_O = 5 V, V_{IC} = 5 V, No load	25°C	Low		2		μA
					High		12		

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.

‡The output will swing to the potential of the ground pin.

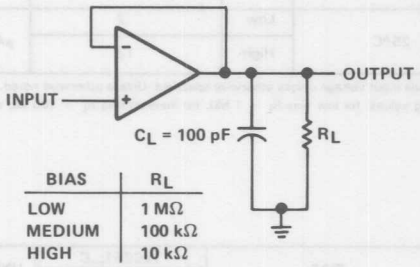
operating characteristics, V_{DD} = 1 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	BIAS	TLC251_C MIN	TLC251_C TYP	TLC251_C MAX	UNIT
B_1	Unity-gain bandwidth	C_L = 10 pF	Low		12		kHz
			High		75		
SR	Slew rate at unity gain	See Figure 1	Low		0.001		V/μs
			High		0.01		
	Overshoot factor	See Figure 1	Low		35%		
			High		30%		

operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	BIAS	TLC2_M			TLC2_I			TLC2_C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF	Low		0.1			0.1			0.1		MHz
			Medium		0.7			0.7			0.7		
			High		2.3			2.3			2.3		
SR	Slew rate at unity gain	See Figure 1	Low		0.04			0.04			0.04		V/μs
			Medium		0.6			0.6			0.6		
			High		4.5			4.5			4.5		
	Overshoot factor	See Figure 1	Low		30%			30%			30%		
			Medium		35%			35%			35%		
			High		35%			35%			35%		
ϕ_m	Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = pF	Low		43°			43°			43°		
			Medium		43°			43°			43°		
			High		50°			50°			50°		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	Low		70			70			70		nV/√Hz
			Medium		38			38			38		
			High		30			30			30		

PARAMETER MEASUREMENT INFORMATION



BIAS	R_L
LOW	1 MΩ
MEDIUM	100 kΩ
HIGH	10 kΩ

FIGURE 1–UNITY-GAIN AMPLIFIER

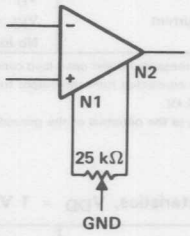


FIGURE 2–INPUT OFFSET VOLTAGE NULL CIRCUIT

SUPPLY CURRENT
vs
BIAS SELECT PIN VOLTAGE

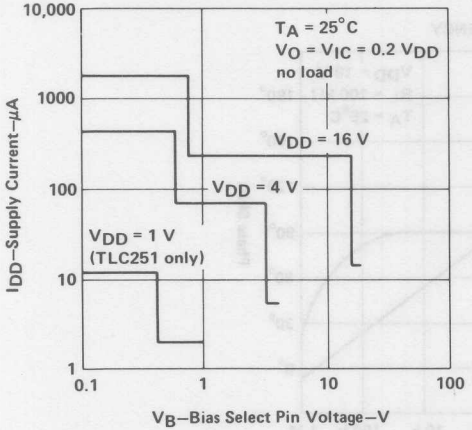


FIGURE 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

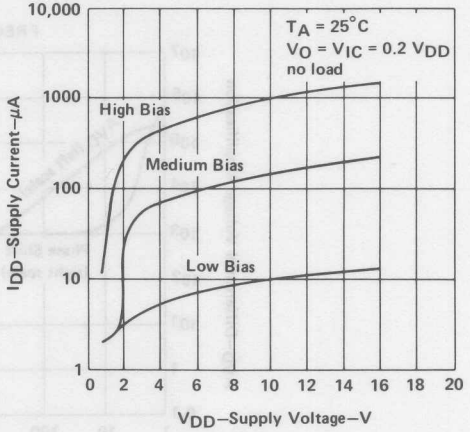


FIGURE 4

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

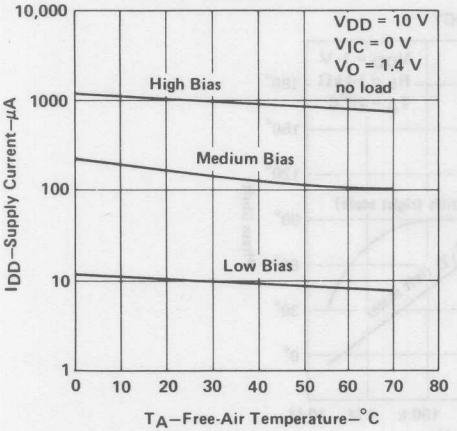


FIGURE 5

LOW BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

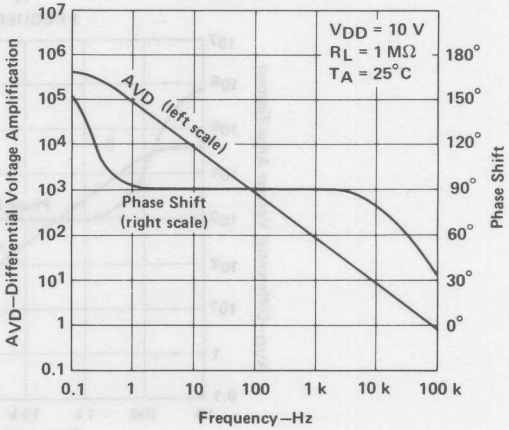


FIGURE 6

TYPICAL CHARACTERISTICS

MEDIUM BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

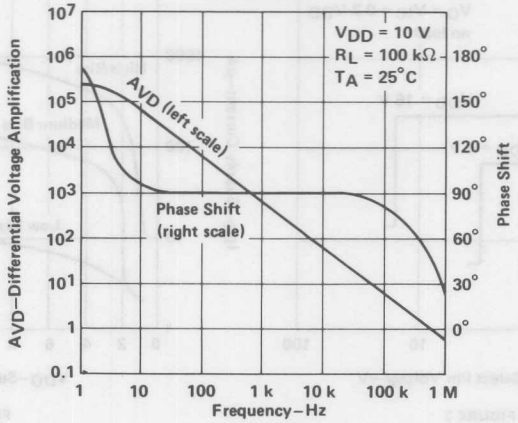


FIGURE 7

HIGH BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

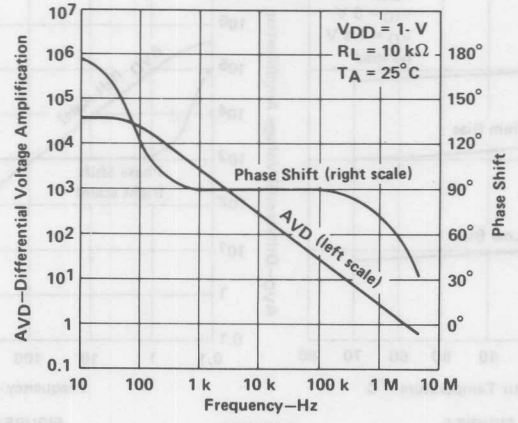


FIGURE 8

TYPICAL APPLICATION INFORMATION

static protection

The inputs of the TLC251 and TLC271 are protected by series resistors and clamp diodes. As with any integrated circuit, ESD handling precautions should be used to avoid damage from strong electrostatic fields.

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be applied simultaneously with, or before, application of any input signals.

using the bias select pin

The TLC251 and TLC271 have a bias select pin that allows the selection of one of three I_{DD} conditions (10, 150, and 1000 μA typical). This allows the user to trade-off power and ac performance. As shown in the typical supply current (I_{DD}) vs supply voltage (V_{DD}) curves (Figure 4), the I_{DD} varies only slightly from 4 to 16 V. Below 4 V, the I_{DD} varies more significantly. Note that the I_{DD} values in the medium and low-bias modes at V_{DD} = 1 V are typically 2 μA, and in the high mode are typically 12 μA. The following table shows the recommended bias select pin connections at V_{DD} = 10 V:

RECOMMENDED BIAS SELECT PIN USE AT V_{DD} = 10 V

BIAS MODE	AC PERFORMANCE	BIAS SELECT CONNECTION†	TYPICAL I_{DD}§
Low	Low	V_{DD}	10 μA
Medium	Medium	0.8 V to 9.2 V	150 μA
High	High	Ground pin	1000 μA

†The Bias Select pin may also be controlled by external circuitry to conserve power, etc. For information regarding the bias select pin, see Figure 3 in the typical characteristics curves.

§For I_{DD} characteristics at voltages other than 10 V, see Figure 4 in the typical characteristics curves.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

input offset nulling

Both the TLC251 and TLC271 offer external offset null control. Nulling may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected to the device GND pin as shown in Figure 2. The amount of nulling range varies with the bias selection. At I_{DD} settings of 150 and 1000 μA (medium and high bias), the nulling range will allow the maximum offset specified to be trimmed to zero. In low bias or when the TLC251 is used below 4 V, total nulling may not be possible on all units.

supply configurations

Even though the TLC251 and TLC271 are characterized for single-supply operation, they can be used effectively in a split-supply configuration when the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

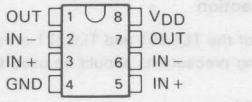
The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive dc leakages.

TYPES TLC252, TLC25L2, TLC25M2, TLC272, TLC27L2, TLC27M2
LinCMOS™ DUAL OPERATIONAL AMPLIFIERS

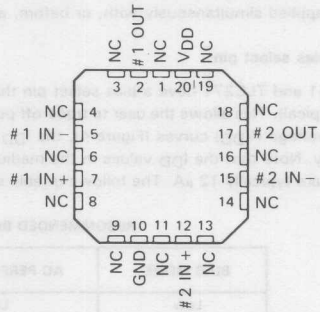
D2752, JUNE 1983

- **Wide Range of Supply Voltages:**
  1 V to 16 V (TLC252 types)
  4 V to 16 V (TLC272 types)
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Includes the Negative Rail**
- **Three Supply Current Ranges Available:**
  TLC25L2 and TLC27L2 . . . 10 μA/Amplifier Typ
  TLC25M2 and TLC27M2 . . . 150 μA/Amplifier Typ
  TLC252 and TLC272 . . . 1000 μA/Amplifier Typ
- **Three Slew-Rate Performances Available:**
  TLC25L2 and TLC27L2 . . . 0.04 V/μs Typ
  TLC25M2 and TLC27M2 . . . 0.6 V/μs Typ
  TLC252 and TLC272 . . . 4.5 V/μs Typ
- **Extremely Low Input Bias and Offset Currents:**
  Input Bias Current . . . 1 pA Typ
  Input Offset Current . . . 1 pA Typ
- **Low Input Offset Voltage . . . 2 mV Max**
- **Ultra-Stable Input Offset Voltage . . .**
  0.1 μV/month Typ
  0.7 μV/°C Typ (Low-Bias Versions)
- **Low Noise. . .30 nV$\sqrt{\text{Hz}}$ Typ at f = 1 kHz (High-Bias Versions)**

D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



TLC272_M. . .FH OR FK PACKAGE
(TOP VIEW)



NC—No internal connection

DEVICE TYPES, SUFFIX VERSIONS, AND PACKAGES

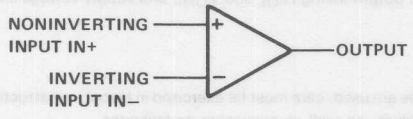
	TLC252__	TLC272__
TLC2__2M	*	JG, FH, FK
TLC2__L4M	*	JG, FH, FK
TLC2__M4M	*	JG, FH, FK
TLC2__2AM	*	JG, FH, FK
TLC2__L2AM	*	JG, FH, FK
TLC2__M2AM	*	JG, FH, FK
TLC2__2BM	*	JG, FH, FK
TLC2__L2BM	*	JG, FH, FK
TLC2__M2BM	*	JG, FH, FK
TLC2__2I	*	JG, P, D
TLC2__L2I	*	JG, P, D
TLC2__M2I	*	JG, P, D
TLC2__2AI	*	JG, P, D
TLC2__L2AI	*	JG, P, D
TLC2__M2AI	*	JG, P, D
TLC2__2BI	*	JG, P, D
TLC2__L2BI	*	JG, P, D
TLC2__M2BI	*	JG, P, D
TLC2__2C	JG, P, D	JG, P, D
TLC2__L2C	JG, P, D	JG, P, D
TLC2__M2C	JG, P, D	JG, P, D
TLC2__2AC	JG, P, D	JG, P, D
TLC2__L2AC	JG, P, D	JG, P, D
TLC2__M2AC	JG, P, D	JG, P, D
TLC2__2BC	JG, P, D	JG, P, D
TLC2__L2BC	JG, P, D	JG, P, D
TLC2__M2BC	JG, P, D	JG, P, D

*These combinations are not defined by this data sheet.

description

The TLC252 and TLC272 series are low-cost, low-power dual operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5 or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. Parts are available with one of the three ac performance and power dissipation levels, from a high level (slew rate of 4.5 V/μs, power

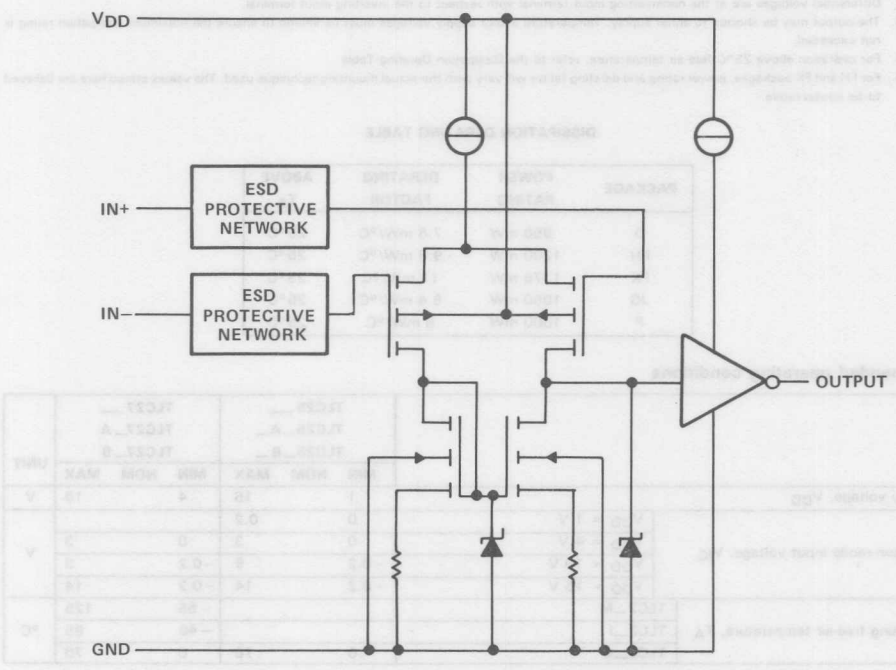
symbol (each amplifier)



dissipation of 20 mW at a supply voltage of 10 volts) to a low level (slew rate of 0.04 V/μs, consuming only 200 μW at 10 volts) to suit the application. The TLC252 types offer the same operation as the TLC272 types, but the TLC252 types also feature guaranteed operation down to a 1-V supply. All devices are unity-gain stable and have excellent noise characteristics.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC252 and TLC272 series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC252 and TLC272 series. Remote and inaccessible equipment applications are possible using the low-voltage and low-power capabilities of the TLC252. The TLC252 types are well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for commercial, industrial, and military temperature ranges and are available in 8-pin plastic and ceramic dual-in-line (DIP) packages, small outline (D) package, and chip carrier (FH, FK) packages.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage range (any input) . . . . . −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . . unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)
D package . . . . . 950 mW
FH package (see Note 5) . . . . . 1200 mW
FK package (see Note 5) . . . . . 1375 mW
JG package . . . . . 1050 mW
P package . . . . . 1000 mW
Operating free-air temperature range: TLC272M . . . . . −55°C to 125°C
TLC272I . . . . . −40°C to 85°C
TLC252C, TLC272C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
4. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table.
5. For FH and FK packages, power rating and derating factor will vary with the actual mounting technique used. The values stated here are believed to be conservative.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	950 mW	7.6 mW/°C	25°C
FH	1200 mW	9.6 mW/°C	25°C
FK	1375 mW	11 mW/°C	25°C
JG	1050 mW	8.4 mW/°C	25°C
P	1000 mW	8 mW/°C	25°C

recommended operating conditions

		TLC25___ TLC25_A_ TLC25_B_			TLC27___ TLC27_A TLC27_B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		1		16	4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1 V	0		0.2				V
	V_{DD} = 4 V	0		3	0		3	
	V_{DD} = 10 V	−0.2		9	−0.2		9	
	V_{DD} = 16 V	−0.2		14	−0.2		14	
Operating free-air temperature, T_A	TLC2_M				−55		125	°C
	TLC2_I				−40		85	
	TLC2_C	0		70	0		70	

M-SUFFIX TYPES

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC272_M			TLC27L2_M			TLC27M2_M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27_M	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				−55°C to 125°C			12			12			12	
		TLC27_AM		25°C			5			5			5	
				−55°C to 125°C			6.5			6.5			6.5	
		TLC27_BM		25°C			2			2			2	
				−55°C to 125°C			3.5			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			−55°C to 125°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				−55°C to 125°C			3000			3000			3000	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				−55°C to 125°C			5000			5000			5000	
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				−55°C to 125°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		30	500		20	280		V/mV
				−55° to 125°C	7			20			10			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = 0, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current (each amplifier)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1000	2000		10	20		150	300	μA
				−55°C to 125°C			3000			35			500	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected form the output to the ground pin.

‡ The output will swing to the potential of the ground pin.

I-SUFFIX TYPES

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC272_I			TLC27L2_I			TLC27M2_I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27_I	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				– 40°C to 85°C			13			13			13	
		TLC27_AI		25°C			5			5			5	
				– 40°C to 85°C			7			7			7	
		TLC27_BI		25°C			2			2			2	
				– 40°C to 85°C			3.5			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			– 40°C to 85°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				– 40°C to 85°C			200			200			200	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				– 40°C to 85°C			300			300			300	
V_{ICR}	Common-mode input voltage range			25°C	–0.2 to 9			–0.2 to 9			–0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				– 40°C to 85°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		30	500		20	280		V/mV
				– 40° to 85°C	7			20			10			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		–55			–55			–55		mA
			V_O = 0, V_{ID} = –100 mV			15			15			15		
I_{DD}	Supply current (each amplifier)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1000	2000		10	20		150	300	μA
				– 40°C to 85°C			2500			40			500	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to the ground pin.

‡ The output will swing to the potential of the ground pin.

C-SUFFIX TYPES

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC252_C, TLC272_C			TLC25L2_C, TLC27L2_C			TLC25M2_C, TLC27M2_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC2_C	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC2_AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC2_BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			0°C to 70°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			100			100			100	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			150			150			150	
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				0°C to 70°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		30	500		20	280		V/mV
				0° to 70°C	7.5			25			15			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = 0, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current (each amplifier)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1000	2000		10	20		150	300	μA
				0°C to 70°C			2100			30			400	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to the ground pin.

‡ The output will swing to the potential of the ground pin.

C-SUFFIX TYPES

electrical characteristics at specified free-air temperature, V_{DD} = 1 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC2_C	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC2_AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC2_BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			0°C to 70°C		1			1			1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			100			100			100	
I_{IB}	Input bias current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			150			150			150	
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C		450			450			450		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common-mode rejection ratio		V_O = 0.2 V, V_{IC} = V_{ICR} min	25°C		77			77			77		dB
I_{DD}	Supply current		No load, V_O = 0.2 V	25°C		12			2			2		μA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected form the output to the ground pin.

‡ The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC252_C TLC272_M TLC272_I TLC272_C			TLC25L2_C TLC27L2_M TLC27L2_I TLC27L2_C			TLC25M2_C TLC27M2_M TLC27M2_I TLC27M2_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		2.3			0.1			0.7		MHz
SR	Slew rate at unity gain	See Figure 1		4.5			0.04			0.6		V/μs
	Overshoot factor	See Figure 1		35%			30%			35%		
ϕ_m	Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = 10 pF		50°			43°			43°		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		30			70			38		$nV\sqrt{Hz}$
V_{o1}/V_{o2}	Cross talk attenuation	A_V = 100		120			120			120		dB

operating characteristics, V_{DD} = 1 V, T_A = 25°C

TEST CONDITIONS		TEST CONDITIONS	TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		75			12			12		kHz
SR	Slew rate at unity gain	See Figure 1		0.01			0.001			0.001		V/μs
	Overshoot factor	See Figure 1		30%			35%			35%		

PARAMETER MEASUREMENT INFORMATION

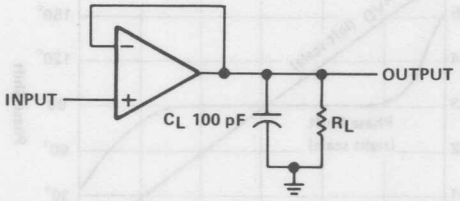


FIGURE 1–UNITY GAIN AMPLIFIER

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

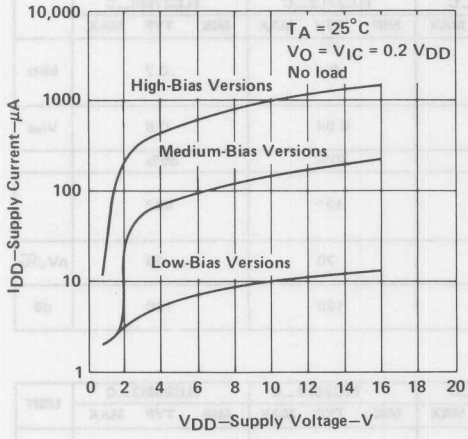


FIGURE 2

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

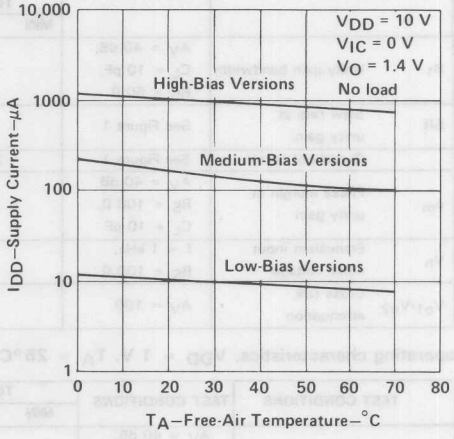


FIGURE 3

LOW-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

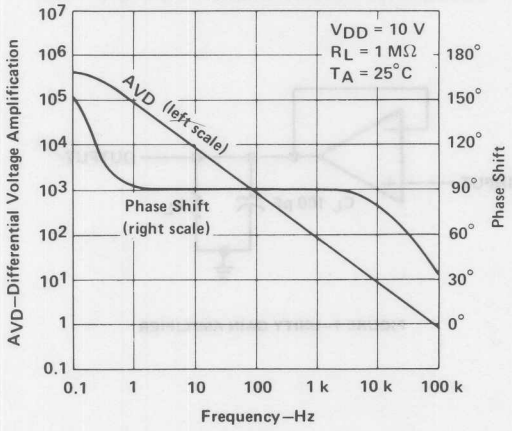


FIGURE 4

TYPICAL CHARACTERISTICS

MEDIUM-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

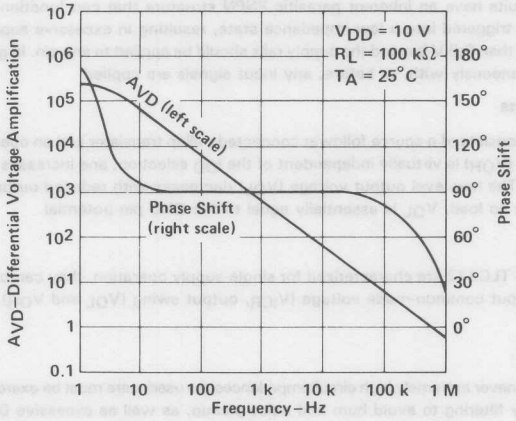


FIGURE 5

HIGH-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

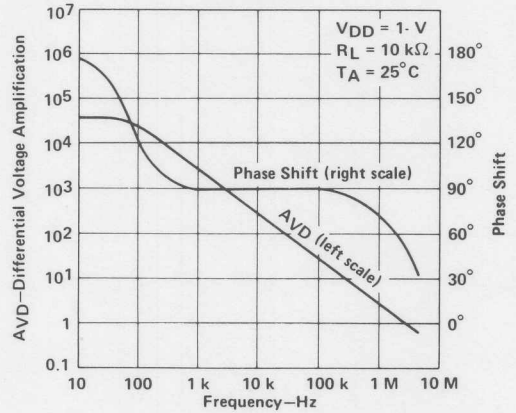


FIGURE 6

TYPICAL APPLICATION INFORMATION

static protection

The inputs of the TLC252 and TLC272 are protected by series resistors and clamp diodes. As with any integrated circuit, ESD handling precautions should be used to avoid damage from strong electrostatic fields.

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be established simultaneously with, or before, any input signals are applied.

output stage considerations

The amplifier's output stage consists of a source follower connected pullup transistor and an open drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

supply configurations

Even though the TLC252 and TLC272 are characterized for single-supply operation, they can be used effectively in a split supply configuration if the input common-mode voltage (V_{ICR}, output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

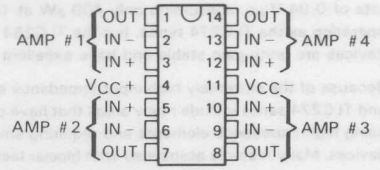
circuit layout precautions

The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive DC leakages.

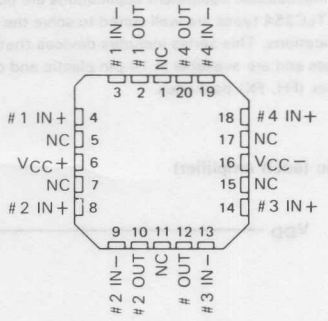
D2753, JUNE 1983

- Wide Range of Supply Voltages:
  1 V to 16 V (TLC254 types)
  4 V to 16 V (TLC274 types)
- True Single-Supply Operation
- Common-Mode Input Voltage Includes the Negative Rail
- Three Supply Current Ranges Available:
  TLC25L4 and TLC27L4. . .10 μA/Amplifier Typ
  TLC25M4 and TLC27M4. . .150 μA/Amplifier Typ
  TLC254 and TLC274. . .1000 μA/Amplifier Typ
- Three Slew-Rate Performances Available:
  TLC25L4 and TLC27L4. . .0.04 V/μs Typ
  TLC25M4 and TLC27M4. . .0.6 V/μs Typ
  TLC254 and TLC274. . .4.5 V/μs Typ
- Extremely Low Input Bias and Offset Currents:
  Input Bias Current. . . 1 pA Typ
  Input Offset Current. . . 1 pA Typ
- Low Input Offset Voltage. . . 2 mV Max
- Ultra-Stable Input Offset Voltage. . .
  0.1 μV/month Typ (Long Term, after 1st month)
  0.7 μV/°C Typ (Low-Bias Versions)
- Low Noise. . .30 nV$\sqrt{\text{Hz}}$ Typ at f = 1 kHz
  (High-Bias Versions)

J, N, OR D DUAL IN-LINE-PACKAGE
(TOP VIEW)



TLC274__M. . .FH OR FK PACKAGE
(TOP VIEW)

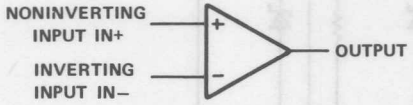


NC – No internal connection

description

The TLC254 and TLC274 series are low-cost, low-power quad operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon-gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5 or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-

symbol (each amplifier)



DEVICE TYPES, SUFFIX VERSIONS, AND PACKAGES

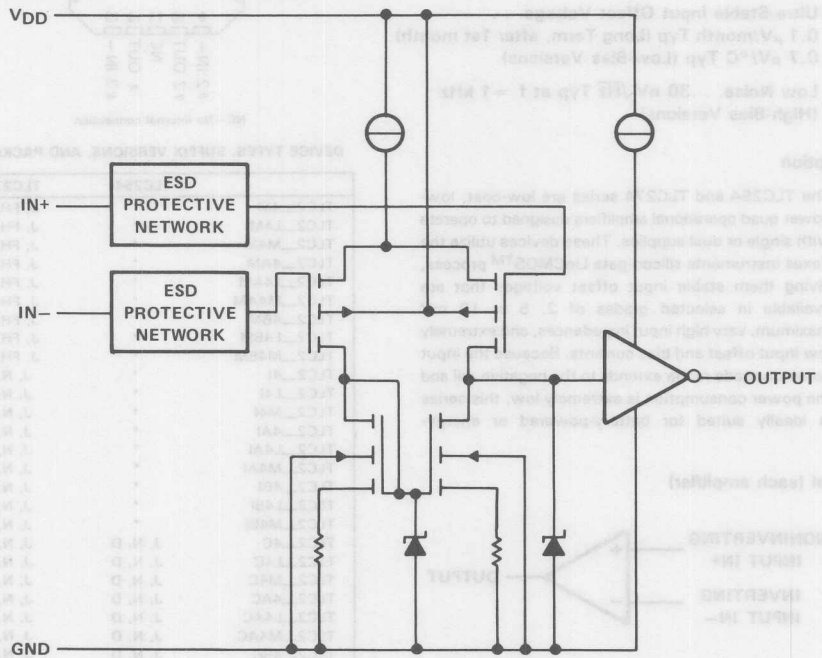
	TLC254	TLC274
TLC2__4M	*	J, FH, FK
TLC2__L4M	*	J, FH, FK
TLC2__M4M	*	J, FH, FK
TLC2__4AM	*	J, FH, FK
TLC2__L4AM	*	J, FH, FK
TLC2__M4AM	*	J, FH, FK
TLC2__4BM	*	J, FH, FK
TLC2__L4BM	*	J, FH, FK
TLC2__M4BM	*	J, FH, FK
TLC2__4I	*	J, N, D
TLC2__L4I	*	J, N, D
TLC2__M4I	*	J, N, D
TLC2__4AI	*	J, N, D
TLC2__L4AI	*	J, N, D
TLC2__M4AI	*	J, N, D
TLC2__4BI	*	J, N, D
TLC2__L4BI	*	J, N, D
TLC2__M4BI	*	J, N, D
TLC2__4C	J, N, D	J, N, D
TLC2__L4C	J, N, D	J, N, D
TLC2__M4C	J, N, D	J, N, D
TLC2__4AC	J, N, D	J, N, D
TLC2__L4AC	J, N, D	J, N, D
TLC2__M4AC	J, N, D	J, N, D
TLC2__4BC	J, N, D	J, N, D
TLC2__L4BC	J, N, D	J, N, D
TLC2__M4BC	J, N, D	J, N, D

*These combinations are not defined by this data sheet.

conserving applications. Parts are available with one of the three ac performance and power dissipation levels, from a high level (slew rate of 4.5 V/μs, power dissipation of 40 mW at a supply voltage of 10 volts) to a low level (slew rate of 0.04 V/μs, consuming only 400 μW at 10 volts) to suit the application. The TLC254 types offer the same operation as the TLC274 types, but the TLC254 types also feature guaranteed operation down to a 1-V supply. All devices are unity-gain stable and have excellent noise characteristics.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC254 and TLC274 series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC254 and TLC274 series. Remote and inaccessible equipment applications are possible using the low-voltage and low-power capabilities of the TLC254. The TLC254 types are well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for commercial, industrial, and military temperature ranges and are available in 14-pin plastic and ceramic dual-in-line (DIP) packages, small outline (D) package, and chip carrier (FH, FK) packages.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage range (any input) . . . . . −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . . unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4):
D package . . . . . 950 mW
FH package (see Note 5) . . . . . 1200 mW
FK package (see Note 5) . . . . . 1375 mW
JG package . . . . . 1375 mW
P package . . . . . 1150 mW
Operating free-air temperature range: TLC274M . . . . . −55°C to 125°C
TLC274I . . . . . −40°C to 85°C
TLC254C, TLC274C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting inp;ut terminal with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation raing is not exceded.
4. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table.
5. For FH and FK packages, power rating and derating factor will vary with the actual mounting technique used. The values stated here are believed to be conservative.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	950 mW	7.6 mW/°C	25°C
FH	1200 mW	9.6 mW/°C	25°C
FK	1375 mW	11 mW/°C	25°C
J	1375 mW	11 mW/°C	25°C
N	1150 mW	9.2 mW/°C	25°C

recommended operating conditions

		TLC25___, TLC25_A__, TLC25_B__			TLC27___, TLC27_A__, TLC27_B__			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		1		16	4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1 V	0		0.2				V
	V_{DD} = 4 V	0		3	0		3	
	V_{DD} = 10 V	−0.2		9	−0.2		9	
	V_{DD} = 16 V	−0.2		14	−0.2		14	
Operating free-air temperature, T_A	TLC2_M				−55		125	°C
	TLC2_I				−40		85	
	TLC2_C	0		70	0		70	

M-SUFFIX TYPES

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC274_M			TLC27L4_M			TLC27M4_M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27_M	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				−55°C to 125°C			12			12			12	
		TLC27_AM		25°C			5			5			5	
				−55°C to 125°C			6.5			6.5			6.5	
		TLC27_BM		25°C			2			2			2	
				−55°C to 125°C			3.5			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			−55°C to 125°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				−55°C to 125°C			3000			3000			3000	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				−55°C to 125°C			5000			5000			5000	
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				−55°C to 125°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		30	500		20	280		V/mV
				−55° to 125°C	7			20			10			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = 0, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current (each amplifier)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1000	2000		10	20		150	300	μA
				−55°C to 125°C			3000			35			500	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected form the output to the ground pin.

‡ The output will swing to the potential of the ground pin.

I-SUFFIX TYPES

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC274_I			TLC27L4_I			TLC27M4_I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27_I	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				– 40°C to 85°C			13			13			13	
		TLC27_AI		25°C			5			5			5	
				– 40°C to 85°C			7			7			7	
		TLC27_BI		25°C			2			2			2	
				– 40°C to 85°C			3.5			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			– 40°C to 85°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				– 40°C to 85°C			200			200			200	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				– 40°C to 85°C			300			300			300	
V_{ICR}	Common-mode input voltage range			25°C	–0.2 to 9			–0.2 to 9			–0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				– 40°C to 85°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		30	500		20	280		V/mV
				– 40° to 85°C	7			20			10			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		–55			–55			–55		mA
			V_O = 0, V_{ID} = –100 mV			15			15			15		
I_{DD}	Supply current (each amplifier)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1000	2000		10	20		150	300	μA
				– 40°C to 85°C			2500			40			500	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to the ground pin.

‡ The output will swing to the potential of the ground pin.

C-SUFFIX TYPES

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC254_C, TLC274_C			TLC25L4_C, TLC27L4_C			TLC25M4_C, TLC27M4_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC2_C	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC2_AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC2_BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			0°C to 70°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			100			100			100	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			150			150			150	
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				0°C to 70°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		30	500		20	280		V/mV
				0° to 70°C	7.5			25			15			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	70	88		70	88		70	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = 0, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current (each amplifier)		No load, V_O = 5 V, V_{IC} = 5 V	25°C		1000	2000		10	20		150	300	μA
				0°C to 70°C			2100			30			400	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to the ground pin.

‡ The output will swing to the potential of the ground pin.

C-SUFFIX TYPES

electrical characteristics at specified free-air temperature, V_{DD} = 1 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC2_C	V_O = 0.2 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC2_AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC2_BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			0°C to 70°C		1			1			1		μV/°C
I_{IO}	Input offset current		V_O = 0.2	25°C		1			1			1		pA
				0°C to 70°C			100			100			100	
I_{IB}	Input bias current		V_O = 0.2	25°C		1			1			1		pA
				0°C to 70°C			150			150			150	
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C		450			450			450		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common-mode rejection ratio		V_O = 0.2 V, V_{IC} = V_{ICR} min	25°C		77			77			77		dB
I_{DD}	Supply current		No load, V_O = 0.2 V	25°C		2			2			2		μA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected form the output to the ground pin.

‡ The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC254_C TLC274_M TLC274_I TLC274_C			TLC25L4_C TLC27L4_M TLC27L4_I TLC27L4_C			TLC25M4_C TLC27M4_M TLC27M4_I TLC27M4_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		2.3			0.1			0.7		MHz
SR	Slew rate at unity gain	See Figure 1		4.5			0.04			0.6		V/μs
	Overshoot factor	See Figure 1		35%			30%			35%		
ϕ_m	Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = 10 pF		50°			43°			43°		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		30			70			38		$nV/\sqrt{Hz}$
V_{O1}/V_{O2}	Cross talk attenuation	A_V = 100		120			120			120		dB

operating characteristics, V_{DD} = 1 V, T_A = 25°C

PARAMETERS		TEST CONDITIONS	TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		75			12			12		kHz
SR	Slew rate at unity gain	See Figure 1		0.01			0.001			0.001		V/μs
	Overshoot factor	See Figure 1		30%			35%			35%		

PARAMETER MEASUREMENT INFORMATION

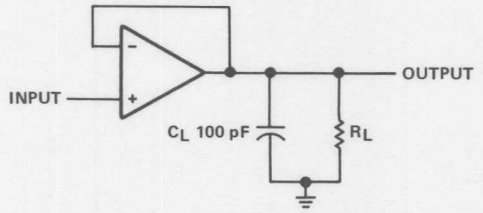


FIGURE 1–UNITY-GAIN AMPLIFIER

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

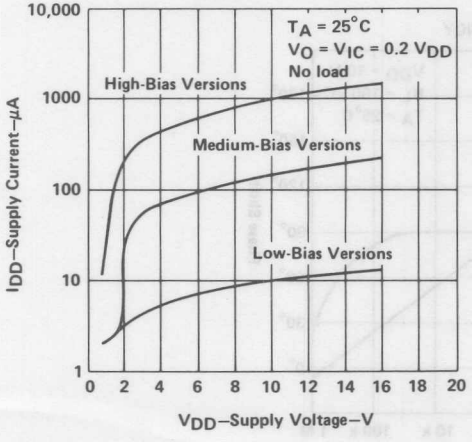


FIGURE 2

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

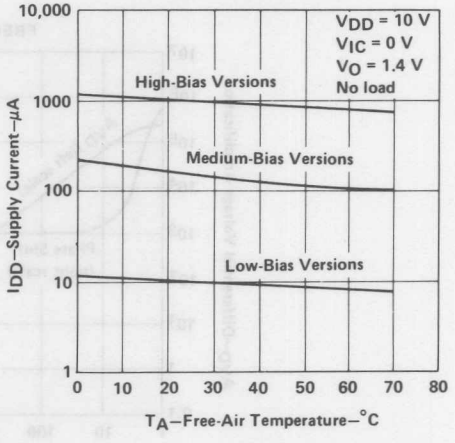


FIGURE 3

LOW-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

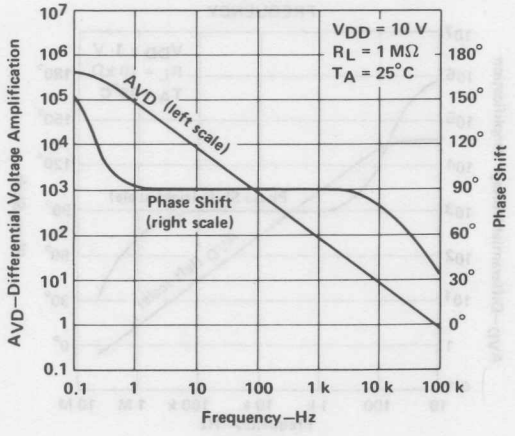


FIGURE 4

TYPICAL CHARACTERISTICS

MEDIUM-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

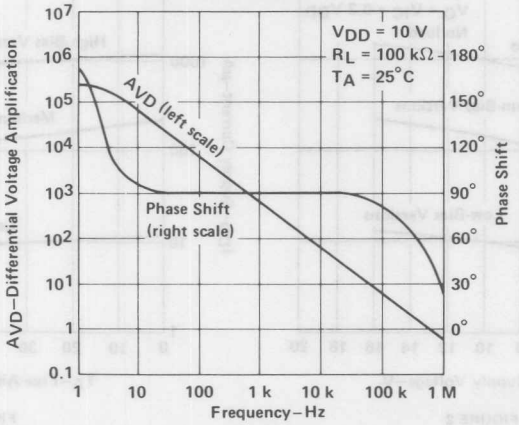


FIGURE 5

HIGH-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

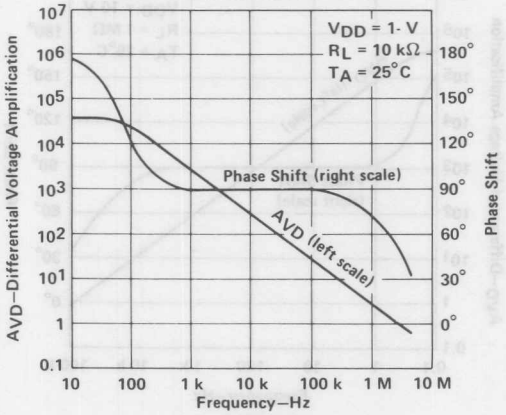


FIGURE 6

TYPICAL APPLICATION INFORMATION

static protection

The inputs of the TLC254 and TLC274 are protected by series resistors and clamp diodes. As with any integrated circuit, ESD handling precautions should be used to avoid damage from strong electrostatic fields.

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be established simultaneously with, or before, any input signals are applied.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

supply configurations

Even though the TLC254 and TLC274 are characterized for single-supply operation, they can be used effectively in a split-supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

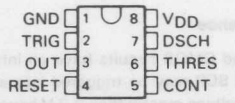
The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive DC leakages.

TYPES TLC555M, TLC555C LinCMOS™ TIMERS

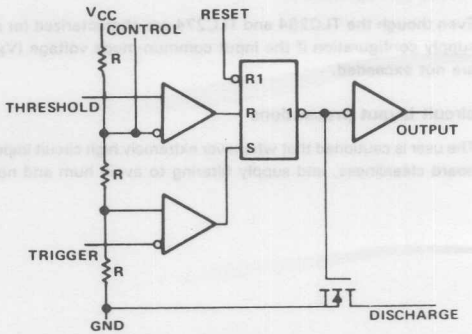
D2784, SEPTEMBER, 1983

- Very Low Power Consumption . . . 1 mW Typ at V_{DD} = 5 V
- Capable of Very High-Speed Operation . . . Typically 2 MHz in Astable Mode
- Complementary CMOS output Capable of Swinging Rail-to-Rail
- High Output-Current Capability
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- Output Fully CMOS-, TTL-, and MOS-Compatible
- Low Supply Current Reduces Spikes During Output Transitions
- High Impedance Inputs . . . 10^{12} Ω Typ
- Single-Supply Operation from 2 to 18 volts
- Functionally Interchangeable with the Signetics NE555; has Same Pinout

TLC555M . . . JG PACKAGE
TLC555C . . . D, JG, or P PACKAGE
(TOP VIEW)



functional block diagram



Reset can override Trigger, which can override Threshold.

description

The TLC555 is a monolithic timing circuit fabricated using TI's LinCMOS™ process. Due to its high-impedance inputs (typically 10^{12} Ω), it is capable of producing accurate time delays and oscillations while using less expensive, smaller timing capacitors than the NE555. Like the NE555, the TLC555 achieves both monostable (using one resistor and one capacitor) and astable (using two resistors and one capacitor) operation. In addition, 50% duty cycle astable operation is possible using only a single resistor and one capacitor. The LinCMOS™ process allows the TLC555 to operate at frequencies up to 2 MHz and be fully compatible with CMOS, TTL, and MOS logic. It also provides very low power consumption (typically 1 mW at V_{DD} = 5 V) over a wide range of supply voltages ranging from 2 volts to 18 volts.

Like the NE555, the threshold and trigger levels are normally two-thirds and one-third respectively of V_{DD}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low impedance path is provided between the discharge terminal and ground.

While the complementary CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC555 exhibits greatly reduced supply current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

The TLC555M is characterized for operation over the full military temperature range of −55°C to 125°C; the TLC555C is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS

FUNCTION TABLE

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	< 1/3 V_{DD}	Irrelevant	High	Off
High	> 1/3 V_{DD}	> 2/3 V_{DD}	Low	On
High	> 1/3 V_{DD}	< 2/3 V_{DD}	As previously established	

†Voltages levels shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to 18 V
Continuous total dissipation at (or below 25°C free-air temperature (see Note 2) . . . . . 600 mW
Operating free-air temperature range: TLC555M . . . . . −55°C to 125°C
TLC555C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 46°C free-air temperature in the D package, derate linearly at the rate of 5.8 mW/°C. In the JG package, TLC555M chips are alloy-mounted.

electrical characteristics at 25°C free-air temperature, V_{DD} = 5 V to 15 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Threshold voltage level as a percentage of supply voltage				66.7%		
Threshold current	V_{DD} = 5 V			10		pA
Trigger voltage level as a percentage of supply voltage				33.3%		
Trigger current	V_{DD} = 5 V			10		pA
Reset voltage level				0.7		V
Reset current	V_{DD} = 5 V			±10		pA
Control voltage (open-circuit) as a percentage of supply voltage				66.7%		
Low-level output voltage	V_{DD} = 15 V	I_{OL} = 10 mA		0.1		V
		I_{OL} = 50 mA		0.5		
		I_{OL} = 100 mA		1		
	V_{DD} = 5 V	I_{OL} = 5 mA		0.1		
		I_{OL} = 8 mA		0.16		
High-level output voltage	V_{DD} = 15 V	I_{OH} = −1 mA		14.8		V
		I_{OH} = −5 mA		14		
		I_{OH} = −10 mA		12.7		
	V_{DD} = 5 V	I_{OH} = −2 mA		4		
		I_{OH} = −1 mA		4.5		
Supply current	V_{DD} = 15 V			360		μA
	V_{DD} = 5 V			170		

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval	V_{DD} = 5 V to 15 V, R_A = R_B = 1 kΩ to 100 kΩ,		1%		
Supply voltage sensitivity of timing interval	C_T = 0.1 μF, See Figure 1		0.1		%/V
Output pulse rise time	V_{DD} = 5 V, R_L = 10 MΩ,		20		ns
Output pulse fall time	C_L = 10 pF		20		
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF		2.1		MHz

TYPICAL APPLICATION DATA

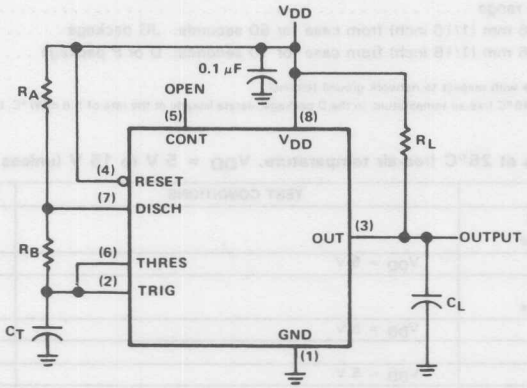


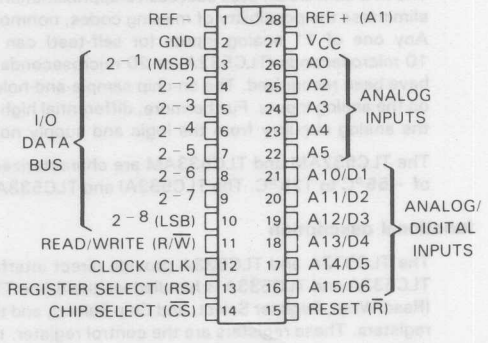
FIGURE 1–CIRCUIT FOR ASTABLE OPERATION

TYPES TLC532AM, TLC532AI, TLC533AM, TLC533AI
LinCMOS™ 8-BIT ANALOG-TO-DIGITAL PERIPHERALS WITH 5 ANALOG AND 6 MULTIPURPOSE INPUTS

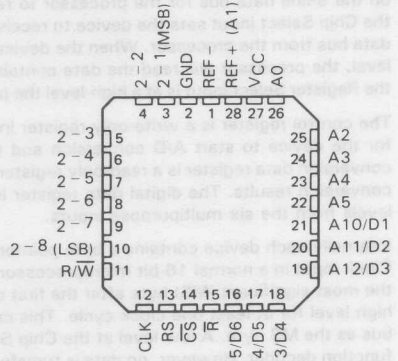
D2819, NOVEMBER 1983

- LinCMOS™ Technology
- 8-Bit Resolution
- Total Unadjusted Error . . . ±0.5 LSB Max
- Ratiometric Conversion
- Access Plus Conversion Time:
  TLC532A. . . 15 μs Max
  TLC533A . . . 30 μs Max
- 3-State, Bidirectional I/O Data Bus
- 5 Analog and 6 Multipurpose Inputs
- On-Chip 12-Channel Analog Multiplexer
- Three On-Chip 16-Bit Data Registers
- Software Compatible with Larger TL530 and TL531 (21-Input Versions)
- On-Chip Sample-and-Hold Circuit
- Single 5-V Supply Operation
- Low Power Consumption . . . 6.5 mW Typ
- Improved Direct Replacements for Texas Instruments TL532 and TL533, National Semiconductor ADC0829, and Motorola MC14442

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FH CHIP-CARRIER PACKAGE
(TOP VIEW)



description

The TLC532A and TLC533A are monolithic LinCMOS™ peripheral integrated circuits each designed to interface a microprocessor for analog data acquisition. These devices are complete peripheral data acquisition systems on a single chip and can convert analog signals to digital data from up to 11 external analog terminals. Each device features operation from a single 5-volt supply. Each contains a 12-channel analog multiplexer, an 8-bit ratiometric analog-to-digital (A/D) converter, a sample-and-hold, three 16-bit registers, and microprocessor-compatible control logic circuitry. Additional features include a built-in self-test, six multipurpose (analog or digital) inputs, five external analog inputs, and an 8-pin input/output (I/O) data port. The three on-chip data registers store the control data, the conversion results, and the input digital data that can be accesssed via the microprocessor data bus in two 8-bit bytes (most-significant byte first). In this manner, a microprocessor can access up to 11 external analog inputs or 6 digital signals and the positive reference voltage that may be used for self-test.

FUNCTION TABLE

ADDRESS/CONTROL					DESCRIPTION
R/W	RS	CS	R	CLK	
X	X	X	L†		Reset
L	H	L	H	↓	Write bus data to control register
H	L	L	H	↑	Read data from analog conversion register
H	H	L	H	↑	Read data from ditigal data register
X	X	H	H	X	No response

H = High-level, L = Low-level, X = Irrelevant,
↓ = High-to-low transition, ↑ = Low-to-high transition
†For proper operation, Reset must be low for at least three clock cycles.

description (continued)

The A/D conversion uses successive-approximation technique and switched-capacitor circuitry. This method eliminates the possibility of missing codes, nonmonotonicity, and a need for zero or full-scale adjustment. Any one of 11 analog inputs (or self-test) can be converted to an 8-bit digital word and stored in 10 microseconds (TLC532A) or 20 microseconds (TLC533A) after instructions from the microprocessor have been recognized. The on-chip sample-and-hold functions automatically to minimize errors due to noise on the analog inputs. Furthermore, differential high-impedance reference inputs are available to help isolate the analog circuitry from the logic and supply noises while easing ratiometric conversion and scaling.

The TLC532AM and TLC533AM are characterized for operation over the full military temperature range of −55°C to 125°C. The TLC532AI and TLC533AI are characterized for operation from −40°C to 85°C.

functional description

The TLC532A and TLC533A provide direct interface to a microprocessor-based system. Control of the TLC532A and TLC533A is handled via the 8-line TTL-compatible 3-state data bus, the three control inputs (Read/Write, Register Select, and Chip Select), and the Clock input. Each device contains three 16-bit internal registers. These registers are the control register, the analog conversion data register, and the digital data register.

A high-level at the Read/Write input and a low-level at the Chip select input sets the device to output data on the 8-line data bus for the processor to read. A low-level at the Read/Write input and a low-level at the Chip Select input sets the device to receive instructions into the internal control register on the 8-line data bus from the processor. When the device is in the read mode and the Register Select input is at low-level, the processor will read the data contained in the analog conversion data register; however, when the Register Select input is at a high-level the processor reads the data contained in the digital data register.

The control register is a write-only register into which the microprocessor writes command instructions for the device to start A/D conversion and to select the analog channel to be converted. The analog conversion data register is a read-only register that contains the current converter status and most recent conversion results. The digital data register is also a read-only register that holds the digital input logic levels from the six multipurpose inputs.

Internally each device contains a byte pointer that selects the appropriate byte during two cycles of the Clock input in a normal 16-bit microprocessor instruction. The internal pointer will automatically point to the most-significant (MS) byte after the first complete clock cycle any time that the Chip Select is at the high level for at least one clock cycle. This causes the device to treat the next signal on the 8-line data bus as the MS byte. A low level at the Chip Select input activates the inputs and outputs and an internal function decoder. However, no data is transferred until the Clock goes high. The internal byte pointer first points to the MS byte of the selected register during the first clock cycle. After the first clock cycle in which the MS byte is accessed, the internal pointer switches to the LS byte and remains there for as long as Chip Select is low. The MS byte of any register may be accessed by either an 8-bit or a 16-bit microprocessor instruction; however, the LS byte may only be accessed by a 16-bit microprocessor instruction.

Normally, a two-byte word is written into or read from the controlling processor, but a single byte can be read by the processor by proper manipulation of the Chip Select input. This can be used to read conversion status from the analog conversion data register or the digital multipurpose input levels from the digital data register. The format and content of each two-byte word is shown in Figures 1 through 3.

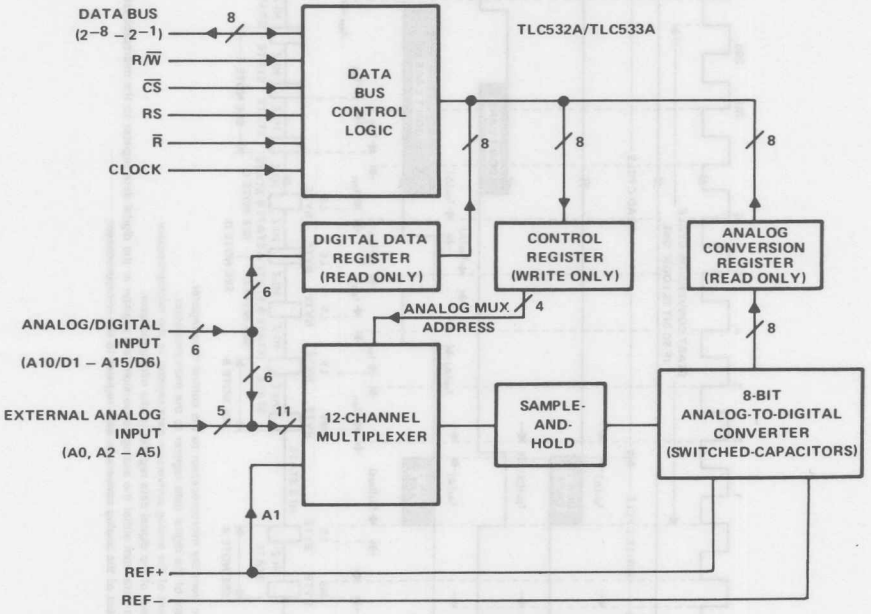
A conversion cycle is started after a two-byte instruction is written into the control register and the start conversion (SC) bit is a logic high. This two-byte instruction also selects the input analog channel to be converted. The status (EOC) bit in the analog conversion data register is reset and it remains at that level until the conversion is completed, at that time the status bit is then set again. After conversion, the results are loaded into the analog conversion data register. These results remain in the analog conversion data

functional description (continued)

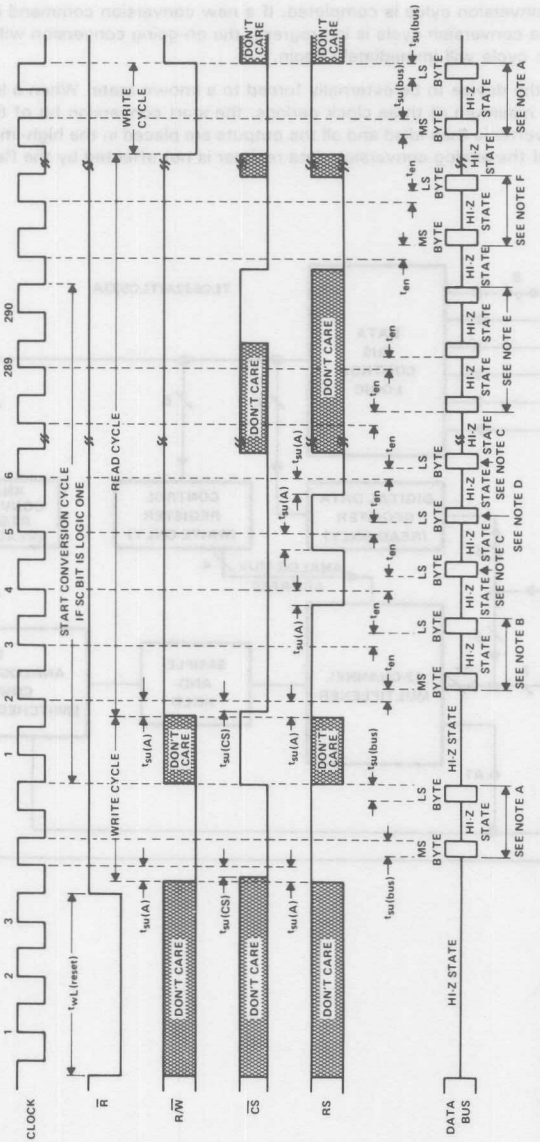
register until the next conversion cylce is completed. If a new conversion command is entered into the control register while the conversion cycle is in progress, the on-going conversion will be aborted and a new channel acquisition cycle will immediately begin.

The Reset input allows the device to be externally forced to a known state. When a low level is applied to the Reset input for a minimum of three clock periods, the start conversion bit of the control register is cleared. The A/D converter is then idled and all the outputs are placed in the high-impedance off-state. However, the content of the analog conversion data register is not affected by the Reset input going to a low level.

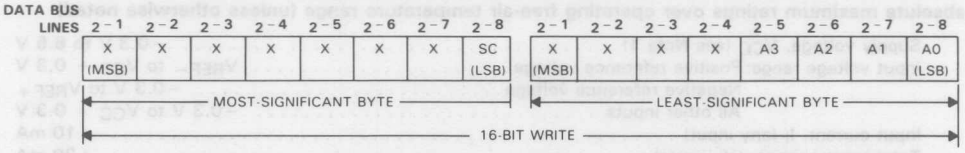
functional block diagram



typical operating sequence



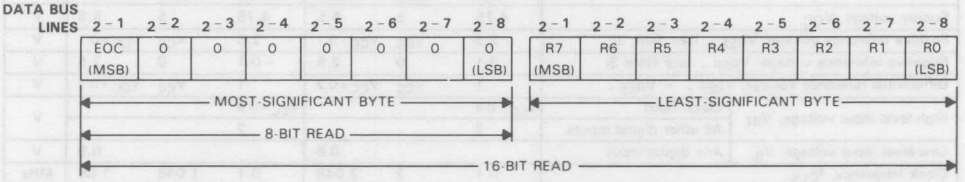
NOTES: A. This is a 16-bit input instruction from the microprocessor to the control data register.
B. this is the 2-byte (16-bit) content of the digital data register to the microprocessor.
C. This is the LS byte (8-bit) content of the analog conversion data register to the microprocessor.
D. This is the LS byte (8-bit) content of the digital data register to the microprocessor.
E. These are 8-bit or 16-bit output data from either the analog conversion data register or the digital data register to the microprocessor.
F. This is the 2-byte (16-bit) content of the analog conversion data register to the microprocessor.



Unused Bits (X) – The MS byte bits 2^{-1} through 2^{-7} and LS byte bits 2^{-1} through 2^{-4} of the control register are not used internally.
Start Conversion (SC) – When the SC bit in the MS byte is set to a logical 1, and analog-to-digital conversion on the specified analog channel will begin immediately after the completion of the control register write.
Analog Multiplex Address (A0-A3) – These four address bits are decoded by the analog multiplexer and used to select the approiate analog channel as shown below:

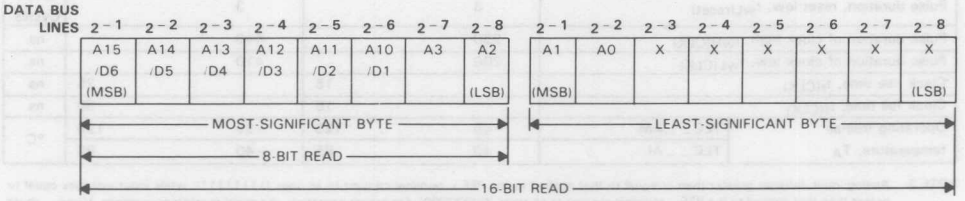
Hexadecimal Address (A3 = MSB)	Channel Select
0	A0
1	REF+ (A1)
2-5	A2-A5
6-9 (not used)	
A-F	A10-A15

FIGURE 1–CONTROL REGISTER TWO-BYTE WRITE WORD FORMAT AND CONTENT



A/D Status (EOC) – The A/D status end-of-conversion (EOC) bit is set whenever an analog-to-digital conversion is successfully completed by the A/D converter. The status bit is cleared by a 16-bit write from the microprocessor to the control register. The remainder of the bits in the MS byte of the analog conversion data register are always set to logical 0 to simplify microprocessor interrogation of the A/D converter status.
A/D Result (R0-R7) – The LS byte of the analog conversion data register contains the result of the analog-to-digital conversion. Result bit R7 is the MSB and the converter follows the standard convention of assigning a code of all ones (11111111) to a full-scale analog voltage. There are no special overflow or underflow indications.

FIGURE 2–ANALOG CONVERSION DATA REGISTER ONE-BYTE AND TWO-BYTE READ WORD FORMAT AND CONTENT



Shared Digital Port (A10/D1-A15/D6) – The voltage present on these pins is interpreted as a digital signal and the corresponding states are read from these bits. A digital value will be given for each pin even if some or all of these pins are being used as analog inputs.
Analog Multiplexer Address (A0-A3) – The address of the selected analog channel presently addressed is given by these bits.
Unused Bits (X) – LS byte bits 2^{-3} through 2^{-8} of the digital data register are not used.

FIGURE 3–DIGITAL DATA REGISTER ONE-BYTE AND TWO-BYTE READ WORD FORMAT AND CONTENT

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 V to 6.5 V
Input voltage range: Positive reference voltage . . . . . V_{REF-} to V_{CC} + 0.3 V
Negative reference voltage . . . . . −0.3 V to V_{REF+}
All other inputs . . . . . −0.3 V to V_{CC} + 0.3 V
Input current, I_I (any input) . . . . . ±10 mA
Total input current, (all inputs) . . . . . ±20 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1375 mW
Operating free-air temperature range: TLC532AM, TLC533AM . . . . . −55°C to 125°C
TLC532AI, TLC533AI . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FH or N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation over 25°C free-air temperature, for N package only, derate linearly to 715 mW at 85°C at the rate of 11 mW/°C.

recommended operating conditions

		TLC532A			TLC533A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 3)		2.5	V_{CC}	$V_{CC}+0.1$	2.5	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 3)		−0.1	0	2.5	−0.1	0	2.5	V
Differential reference voltage, $V_{REF+} - V_{REF-}$		1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
High-level input voltage, V_{IH}	Clock input	$V_{CC}-0.8$			$V_{CC}-0.8$			V
	All other digital inputs	2			2			
Low-level input voltage, V_{IL}	Any digital input			0.8			0.8	V
Clock frequency, f_{CLK}		0.1	2	2.048	0.1	1.048	1.06	MHz
$\overline{CS}$ setup time, $t_{su(CS)}$		75			100			ns
Address (R/$\overline{W}$ and RS) setup time, $t_{su(A)}$		100			145			ns
Data bus input setup time, $t_{su(bus)}$		140			185			ns
Control (R/$\overline{W}$, RS, and $\overline{CS}$) hold time, $t_{h(C)}$		10			20			ns
Data bus input hold time, $t_{h(bus)}$		15			20			ns
Pulse duration of control during read, $t_{w(C)}$		305			575			ns
Pulse duration, reset low, $t_{wL(reset)}$		3			3			Clock Cycles
Pulse duration of clock high, $t_{wH(CLK)}$		230			440			ns
Pulse duration of clock low, $t_{wL(CLK)}$		200			410			ns
Clock rise time, $t_{r(CLK)}$				15			25	ns
Clock fall time, $t_{f(CLK)}$				16			30	ns
Operating free-air temperature, T_A	TLC_ _AM	−55		125	−55		125	°C
	TLC_ _AI	−40		85	−40		85	

NOTE 3: Analog input voltages greater than or equal to that applied to the REF+ terminal convert to all ones (11111111), while input voltages equal to or less than that applied to the REF− terminal convert to all zeros (00000000). For proper operation, the positive reference voltage, V_{REF+}, must be at least 1-volt greater than the negative reference voltage, V_{REF-}. In addition, unadjusted errors may increase as the differential reference voltage, $V_{REF+} - V_{REF-}$, falls below 4.75 volts.

electrical characteristics over recommended operating free-air temperature range, V_{REF+} = V_{CC}, V_{REF-} at ground, f_{CLK} = 2 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1.6 mA	2.4			V
V_{OL}	low-level output voltage		I_{OL} = 1.6 mA			0.4	V
I_{IH}	High-level input current	Any digital or Clock input	V_{IH} = 5.5 V			10	μA
		Any control input				1	
I_{IL}	Low-level input current	Any digital or Clock input	V_{IL} = 0			−10	μA
		Any control input				−1	
I_{OZ}	Off-state (high impedance-state) output current		$V_O = V_{CC}$			10	μA
			V_O = 0			−10	
I_I	Analog input current (see Note 4)		V_I = 0 V to V_{CC}			±500	nA
	Leakage current between selected channel and all other analog channels		V_I = 0 V to V_{CC}, Clock input at 0			±400	nA
C_i	Input capacitance	Digital pins 3 thru 10			4	30	pF
		All other input pins			2	15	
$I_{CC} + I_{REF+}$	Supply current plus reference current		$V_{CC} = V_{REF+}$ = 5.5 V, Outputs open		1.5	3	mA
I_{CC}	Supply current		V_{CC} = 5.5 V		1.4	2	mA

NOTE 4: Analog input current is an average of the current flowing into a selected analog channel input during one full conversion cycle.

operating characteristics over recommended operating free-air temperature range, V_{REF+} = V_{CC}, V_{REF-} at ground, f_{CLK} = 2 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Linearity error		(See Note 5)			±0.5	LSB
	Zero error		(See Note 6)			±0.5	LSB
	Full-scale error		(See Note 6)			±0.5	LSB
	Total unadjusted error		(See Note 7)			±0.5	LSB
	Absolute accuracy error		(See Note 8)			±1	LSB
t_{conv}	Conversion time (including channel acquisition time)				30		Clock Cycles
t_{acq}	Channel acquisition time				10		Clock Cycles
t_{en}	Data output enable time		C_L = 50 pF, R_L = 3 kΩ, (See Note 9)			250	ns
t_{dis}	Data output disable time		C_L = 50 pF, R_L = 3 kΩ	10			ns
$t_{r(bus)}$	Data bus output rise time	High-impedance to high-level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		Low to high-level				300	
$t_{f(bus)}$	Data bus output fall time	High-impedance to low-level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		High to low-level				300	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 5. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
6. Zero error is the difference between the output of an ideal and an actual A/D for zero input voltage; full-scale error is that same difference for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
8. Absolute accuracy error is the maximum difference between an analog value and the nominal midstep value within any step. This includes all errors including inherent quantization error, which is the ±0.5 LSB uncertainty caused by the A/D converters finite resolution.
9. If chip-select setup time, $t_{su(CS)}$, is less than 0.14 microseconds, the effective data output enable time, t_{en}, may extend such that $t_{su(CS)} + t_{en}$ is equal to a maximum of 0.475 microseconds.

electrical characteristics over recommended ranges of V_{CC}, V_{REF+}, and operating free-air temperature, V_{REF-} at ground, f_{CLK} = 1.048 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1.6 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 1.6 mA			0.4	V
I_{IH}	High-level input current	Any digital or Clock input	V_{IH} = 5.5 V			10	μA
		Any control input				1	
I_{IL}	Low-level input current	Any digital or Clock input	V_{IL} = 0			−10	μA
		Any control input				−1	
I_{OZ}	Off-state (high impedance-state) output current		$V_O = V_{CC}$			10	μA
			V_O = 0			−10	
I_I	Analog input current (see Note 4)		V_I = 0 V to V_{CC}			±500	nA
	Leakage current between selected channel and all other analog channels		V_I = 0 V to V_{CC}, Clock input at 0			±400	nA
C_i	Input capacitance	Digital pins 3 thru 10			4	30	pF
		All other input pins			2	15	
$I_{CC} + I_{REF+}$	Supply current plus reference current		$V_{CC} = V_{REF+}$ = 5.5 V, Outputs open		1.3	3	mA
I_{CC}	Supply current		V_{CC} = 5.5 V		1.2	2	mA

NOTE 4: Analog input current is an average of the current flowing into a selected analog channel input during one full conversion cycle.

operating characteristics over recommended ranges of V_{CC}, V_{REF+}, and operating free-air temperature, V_{REF-} at ground, f_{CLK} = 1.048 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Linearity error		(See Note 5)			±0.5	LSB
	Zero error		(See Note 6)			±0.5	LSB
	Full-scale error		(See Note 6)			±0.5	LSB
	Total unadjusted error		(See Note 7)			±0.5	LSB
	Absolute accuracy error		(See Note 8)			±1	LSB
t_{conv}	Conversion time (including channel acquisition time)				30		Clock Cycles
t_{acq}	Channel acquisition time				10		Clock Cycles
t_{en}	Data output enable time		C_L = 50 pF, R_L = 3 kΩ, (See Note 9)			335	ns
t_{dis}	Data output disable time		C_L = 50 pF, R_L = 3 kΩ	10			ns
$t_{r(bus)}$	Data bus output rise time	High-impedance to high-level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		Low to high-level				300	
$t_{f(bus)}$	Data bus output fall time	High-impedance to low-level	C_L = 50 pF, R_L = 3 kΩ			150	ns
		High to low-level				300	

†Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 5. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
6. Zero error is the difference between the output of an ideal and an actual A/D for zero input voltage; full-scale error is that same difference for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero, and full-scale errors.
8. Absolute accuracy error is the maximum difference between an analog value and the nominal midstep value within any step. This includes all errors including inherent quantization error, which is the ±0.5 LSB uncertainty caused by the A/D converters finite resolution.
9. If chip-select setup time, $t_{su(CS)}$, is less than 0.14 microseconds, the effective data output enable time, t_{en}, may extend such that $t_{su(CS)} + t_{en}$ is equal to a maximum of 0.475 microseconds.

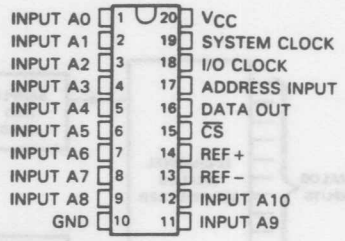
TYPES TLC540M, TLC540I, TLC541M, TLC541I
8-BIT ANALOG-TO-DIGITAL PERIPHERALS WITH SERIAL CONTROL AND 11 INPUTS

D2799, OCTOBER 1983

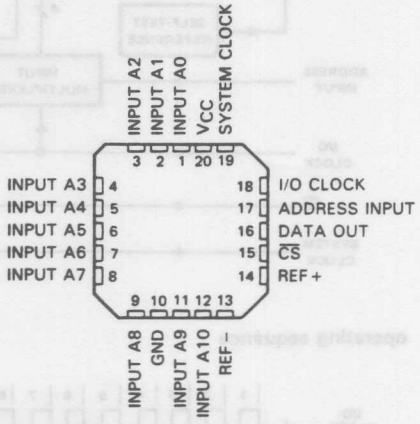
- LinCMOS™ Technology
- 8-Bit Resolution A/D Converter
- On-Chip 12-Channel Analog Multiplexer
- Built-In Self-Test Mode
- Software-Controllable Sample and Hold
- Total Unadjusted Error . . . ±0.5 LSB Max
- Direct Replacement for Motorola MC145040

TYPICAL PERFORMANCE:	TLC540	TLC541
Channel Acquisition Time	2 μs	7 μs
Conversion Time	10 μs	19 μs
Sampling Rate	71 × 10^3	29 × 10^3
Power Dissipation	6 mW	6 mW

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



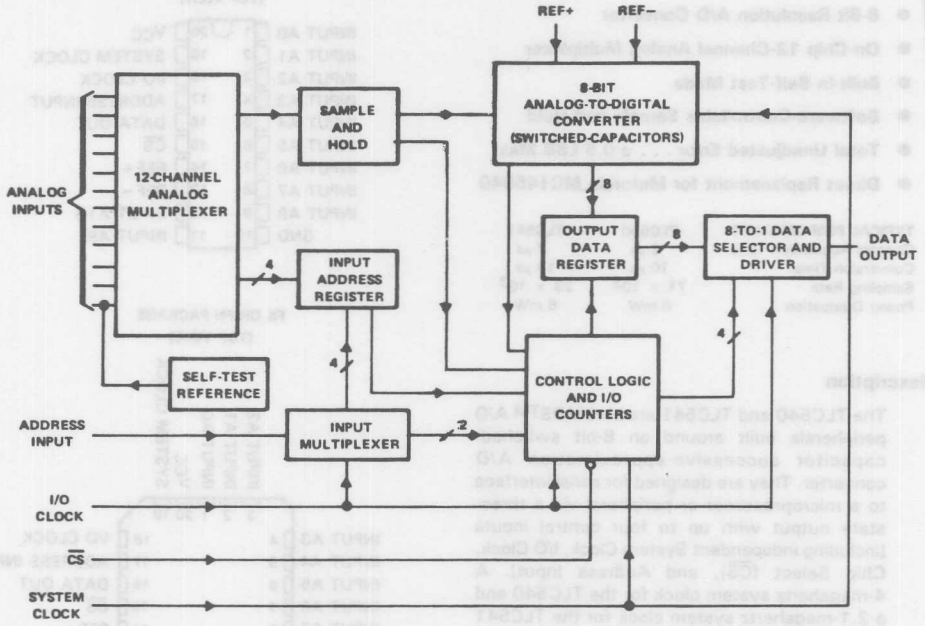
description

The TLC540 and TLC541 are LinCMOS™ A/D peripherals built around an 8-bit switched-capacitor successive-approximation A/D converter. They are designed for serial interface to a microprocessor or peripheral via a three-state output with up to four control inputs [including independent System Clock, I/O Clock, Chip Select ($\overline{CS}$), and Address Input]. A 4-megahertz system clock for the TLC540 and a 2.1-megahertz system clock for the TLC541 with a design that includes simultaneous read/write operation allow high-speed data transfers and sample rates of up to 71,910 samples per second for the TLC540 and 29,144 samples per second for the TLC541. In addition to the high-speed converter and versatile control logic, there is an on-chip 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal "self-test" voltage, and a sample-and-hold that can operate automatically or under processor control.

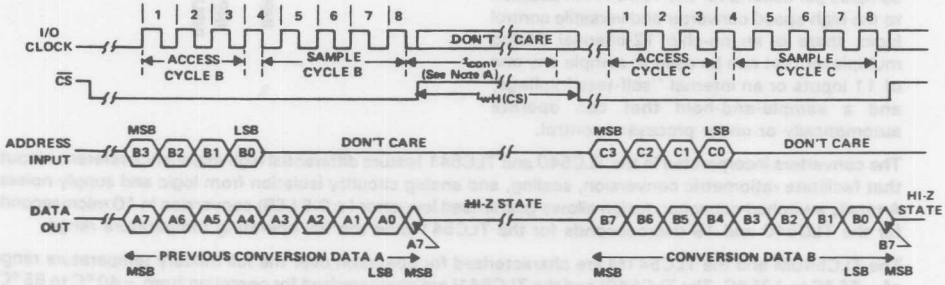
The converters incorporated in the TLC540 and TLC541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched-capacitor design allows guaranteed low-error (±0.5 LSB) conversion in 10 microseconds for the TLC540 and 19 microseconds for the TLC541 over the full operating temperature range.

The TLC540M and the TLC541M are characterized for operation over the full military temperature range of −55°C to 125°C. The TLC540I and the TLC541I are characterized for operation from −40°C to 85°C.

functional block diagram



operating sequence



NOTE A: The conversion cycle, which requires 40 system clock periods, is initiated with the 8th I/O clock ↓ after CS ↓ for the channel whose address exists in memory at that time.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range (any input) . . . . . −0.3 V to V_{CC} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} + 0.3 V
Peak input current range (any input) . . . . . ±10 mA
Peak total input current (all inputs) . . . . . ±30 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 875 mW
Operating free-air temperature range: TLC540I, TLC541I . . . . . −40°C to 85°C
TLC540M, TLC541M . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FN or N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to digital ground with REF− and GND wired together (unless otherwise noted).
2. For operation above 25°C free-air temperature, see Dissipation Derating Curves, Section 2. In the J package, TLC540M and TLC541M chips are alloy mounted, TLC540I and TLC541I chips are glass mounted.

recommended operating conditions

			TLC540			TLC541			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 3)			1.25	V_{CC}	$V_{CC}+0.1$	1.25	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 3)			−0.1	0	$V_{CC}-1.25$	0.1	0	$V_{CC}-1.25$	V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 3)			1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 3)			0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}			2			2			V
Low-level control input voltage, V_{IL}					0.8			0.8	V
Setup time, address bits at data input before I/O CLK↑, $t_{su(A)}$			200			400			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 4)			2			2			System clock cycles
Input/Output clock frequency, $f_{CLK(I/O)}$			0.005		2.048	0		0.525	MHz
System clock frequency, $f_{CLK(SYS)}$			$f_{CLK(I/O)}$			$f_{CLK(I/O)}$			MHz
System clock high, $t_{wH(SYS)}$			110			210			ns
System clock low, $t_{wL(SYS)}$			100			190			ns
Input/Output clock high, $t_{wH(I/O)}$			200			808			ns
Input/Output clock low, $t_{wL(I/O)}$			200			808			ns
Clock transition time (see Note 5)	System	$f_{CLK(SYS)} \le 1048$ kHz			30			30	ns
		$f_{CLK(SYS)} > 1048$ kHz			20			20	
	I/O	$f_{CLK(I/O)} \le 525$ kHz			100			100	ns
		$f_{CLK(I/O)} > 525$ kHz			40			40	
Operating free-air temperature, T_A		TLC540M, TLC541M	−55		125	−55		125	°C
		TLC540I, TLC541I	−40		85	−40		85	

NOTES: 3. Analog input voltages greater than that applied to REF+ convert as all "1"s (11111111), while input voltages less than that applied to REF− convert as all "0"s (00000000). For proper operation, REF+ voltage must be at least 1 volt higher than REF− voltage. Also, adjusted errors may increase as this differential reference voltage falls below 4.75 volts.
4. To minimize errors caused by noise at the Chip Select input, the internal circuitry waits for two system clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the chip select setup time has elapsed.
5. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min.

electrical characteristics over recommended operating temperature range, $V_{CC} = V_{REF+} = 4.75$ V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)} = 2.028$ MHz for TLC540 or $f_{CLK(I/O)} = 0.525$ MHz for TLC541

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 16)		V_{CC} = 4.75 V, I_{OH} = 360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V, I_O = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		$V_O = V_{CC}$, $\overline{CS}$ at V_{CC}			10	μA
			V_O = 0, $\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		$V_I = V_{CC} + 0.3$ V		0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0		−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V		1.2	2	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V		0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}		−0.4	−1	
$I_{CC} + I_{REF}$	Supply and reference current		$V_{REF+} = V_{CC}$, $\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs			7	55	pF
		Control inputs			5	15	

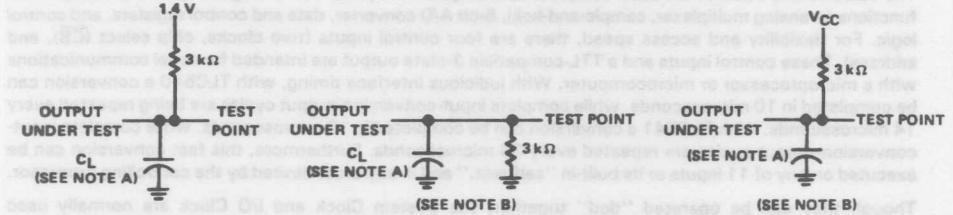
†All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{REF+} = 4.75$ V to 5.5 V, $f_{CLK(I/O)} = 2.048$ MHz for TLC540 or 0.525 MHz for TLC541, $f_{CLK(SYS)} = 4$ MHz for TLC540 or 2.097 MHz for TLC541.

	PARAMETER	TEST CONDITIONS	TLC540			TLC541			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Linearity error	See Note 6			±0.5			±0.5	LSB
	Zero error	See Note 7			±0.5			±0.5	LSB
	Full-scale error	See Note 7			±0.5			±0.5	LSB
	Total unadjusted error	See Note 8			±0.5			±0.5	LSB
	Self-test output code	Input address = 1011 (A11) (See Note 9)	01111101 (125)		10000011 (131)	01111101 (125)		10000011 (131)	
t_{conv}	Conversion time				10			19	μs
t_{acq}	Channel acquisition time				4			4	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓		10			10			ns
t_d	Delay time, I/O clock↓ to data output valid				200			400	ns
t_{acc}	Output access time (delay to valid output after chip select↓)	See Parameter Measurement Information	1		3	1		3	System clock cycles
t_{en}	Output enable time				150			150	ns
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

NOTES: 6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Zero Error is the difference between the output of an ideal and an actual A/D for zero input voltage; full-scale error is that same difference for full-scale input voltage.
8. Total Unadjusted Error is the sum of linearity, zero, and full-scale errors.
9. Both the input address and the output codes are expressed in positive logic.

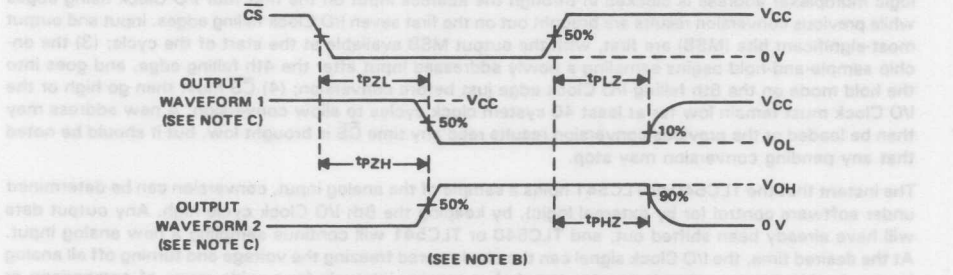
PARAMETER MEASUREMENT INFORMATION



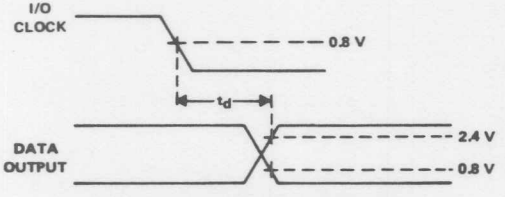
LOAD CIRCUIT FOR t_d, t_{acc}, t_r, t_f

LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}

LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME

VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC540 and 100 pF for TLC541

B. t_{en} = t_{PZH} or t_{PZL}, t_{dis} = t_{PHZ} or t_{PLZ}

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

principles of operation

The TLC540 and TLC541 are each complete data acquisition systems on a single chip. They include such functions as analog multiplexer, sample-and-hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs [two clocks, chip select ($\overline{CS}$), and address]. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. With judicious interface timing, with TLC540 a conversion can be completed in 10 microseconds, while complete input-conversion-output cycles are being repeated every 14 microseconds. With TLC541 a conversion can be completed in 19 microseconds, while complete input-conversion-output cycles are repeated every 35 microseconds. Furthermore, this fast conversion can be executed on any of 11 inputs or its built-in "self-test," and in any order desired by the controlling processor.

Though they can be operated "tied" together, the System Clock and I/O Clock are normally used independently, with no special phase or speed relationship to be considered. This allows integrated circuit operation to continue independent of serial Input/Output timing, permitting manipulation of the I/O Clock as desired for a wide range of software and hardware needs.

The I/O Clock, Data Input, and Data Output are controlled by $\overline{CS}$. It floats the 3-state output and shuts off signals to other control inputs while it is high. This allows any pins except pin 15 to share lines with other integrated circuits. A normal control sequence is as follows: (1) $\overline{CS}$ goes low; (2) a new positive-logic multiplexer address is clocked in through the address input on the first four I/O Clock rising edges while previous conversion results are brought out on the first seven I/O Clock falling edges. Input and output most-significant bits (MSB) are first, with the output MSB available at the start of the cycle; (3) the on-chip sample-and-hold begins sampling a newly addressed input after the 4th falling edge, and goes into the hold mode on the 8th falling I/O Clock edge just before conversion; (4) $\overline{CS}$ must then go high or the I/O Clock must remain low for at least 40 system clock cycles to allow conversion. A new address may then be loaded or the previous conversion results read any time $\overline{CS}$ is brought low, but it should be noted that any pending conversion may stop.

The instant that the TLC540 or TLC541 holds a sample of the analog input, conversion can be determined under software control (or by external logic), by keeping the 8th I/O Clock cycle high. Any output data will have already been shifted out, and TLC540 or TLC541 will continue sampling a new analog input. At the desired time, the I/O Clock signal can then be lowered freezing the voltage and turning off all analog inputs. In this manner, signals can be sampled at precise intervals for a wide range of comparison or processing applications, in much the same manner as a strobe light is used to determine engine speed.